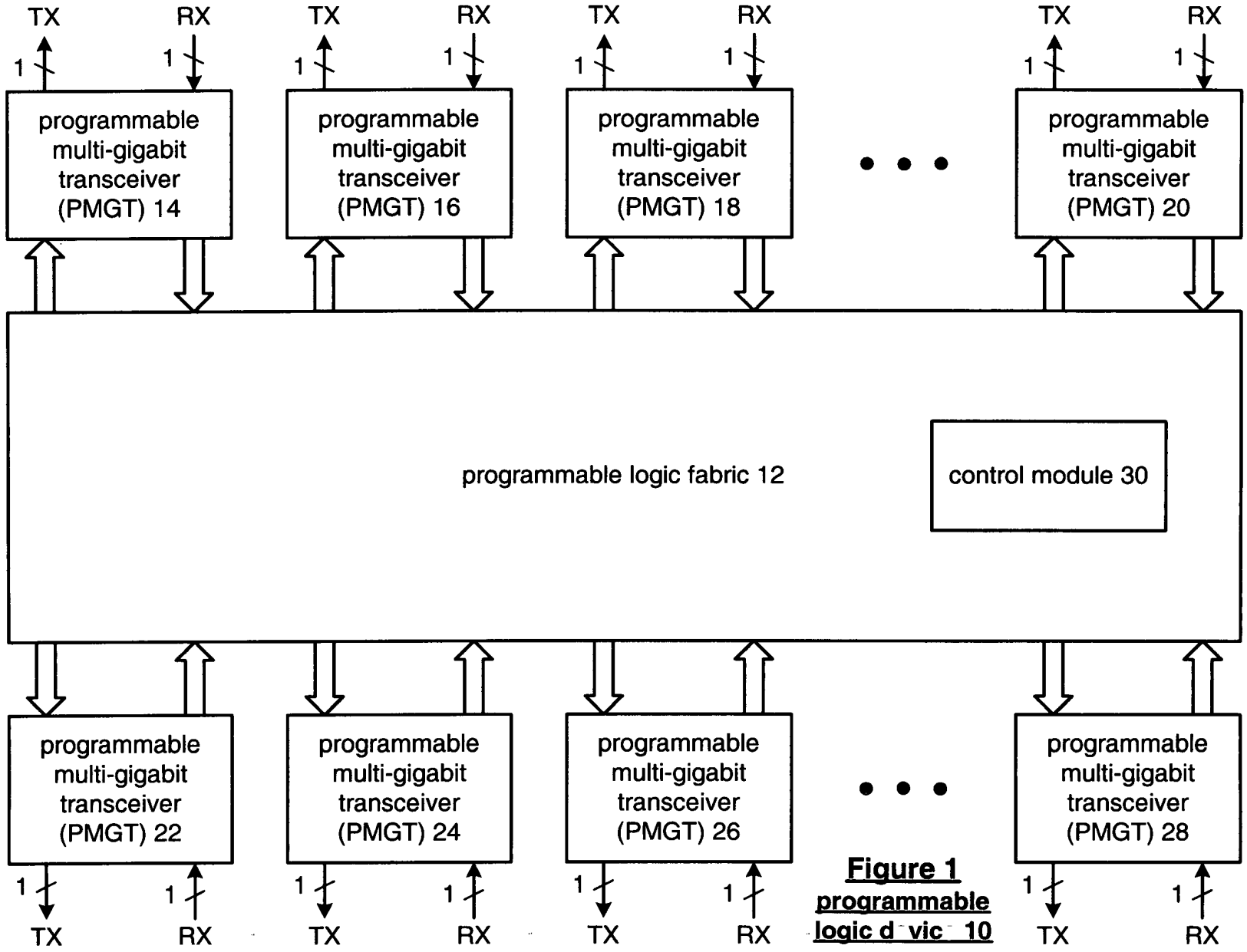


Figure 1
programmable logic d vic 10

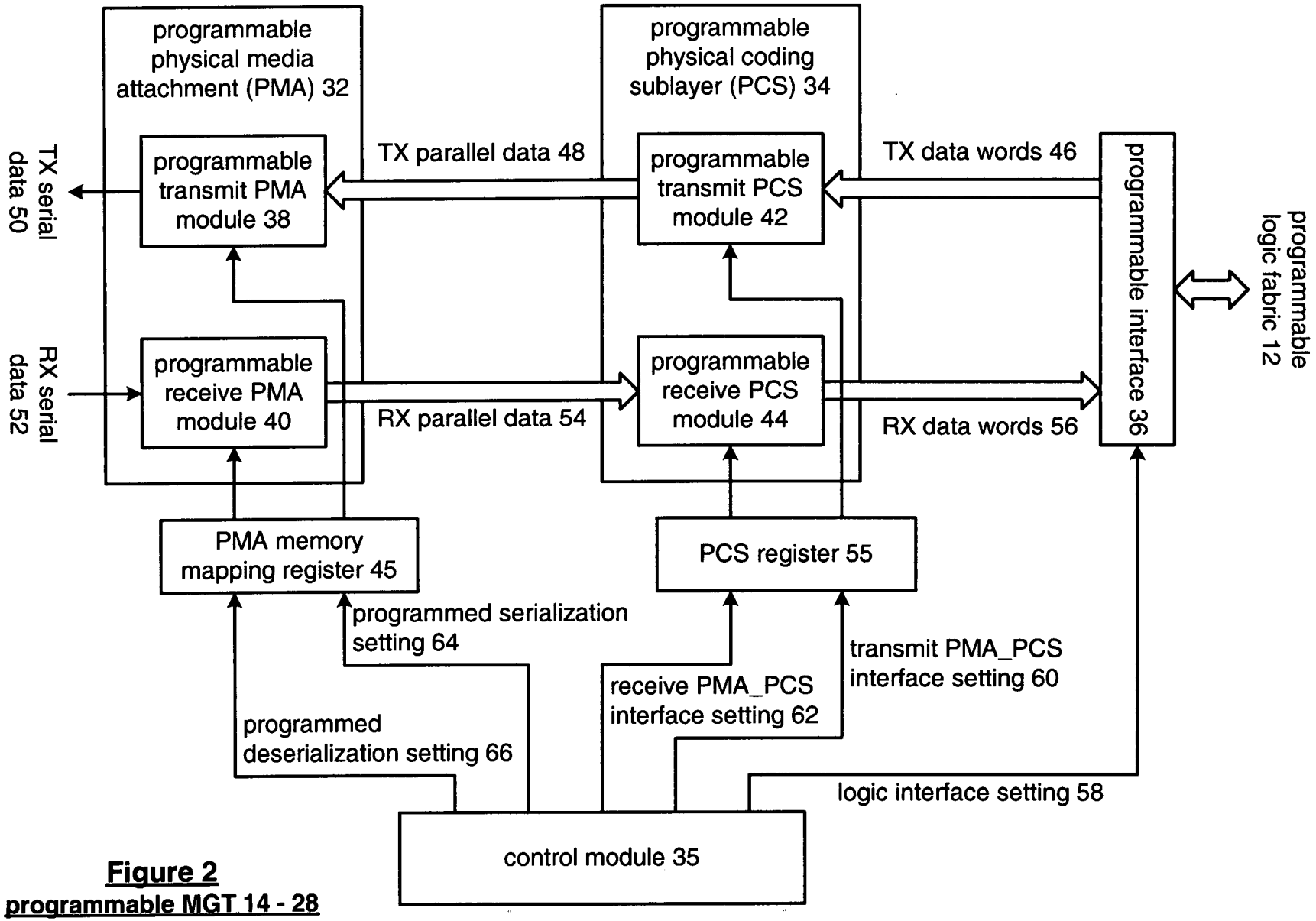


Figure 2
programmable MGT 14 - 28

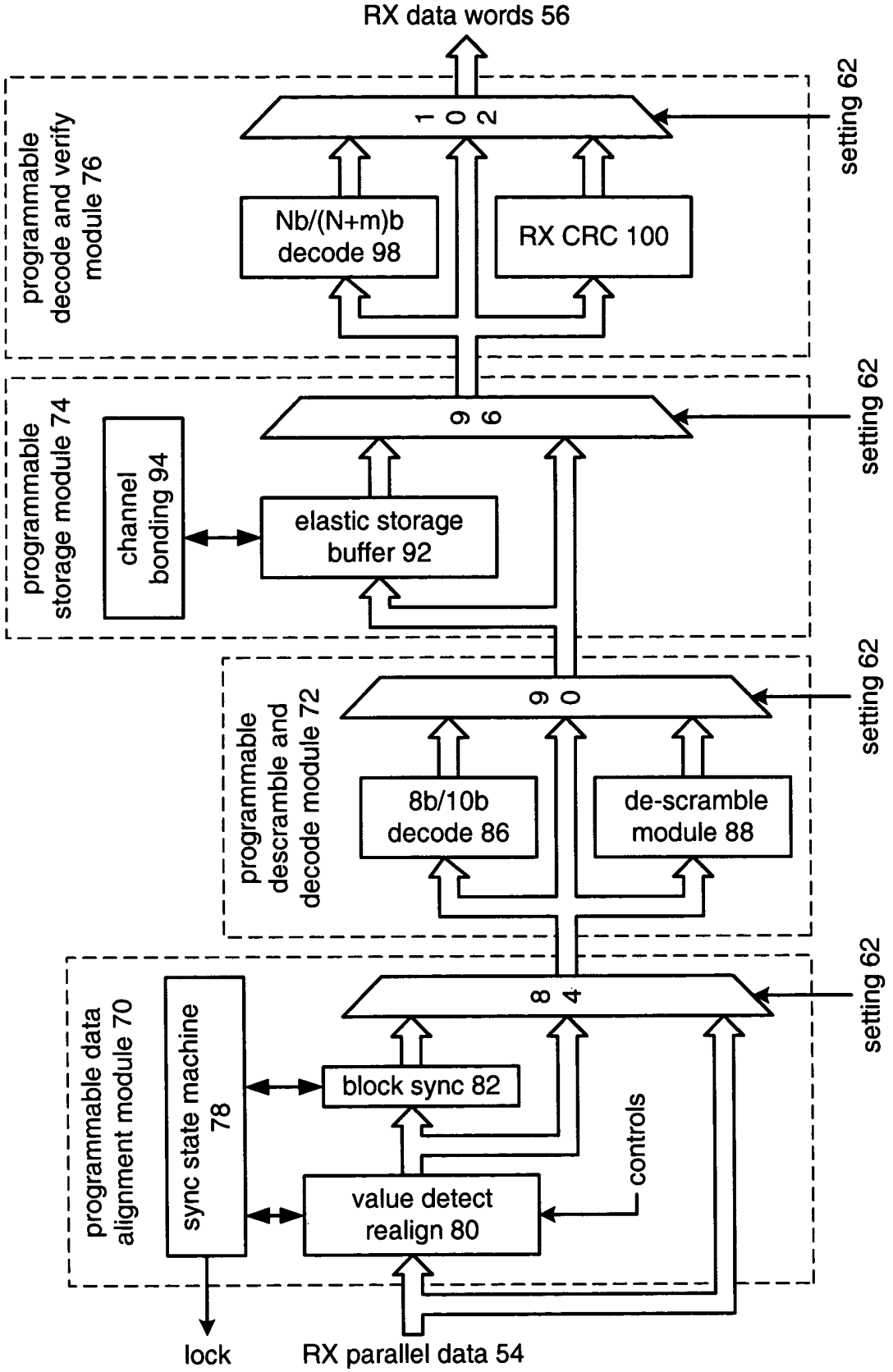


Figure 3
programmabl r c iv PCS module 44

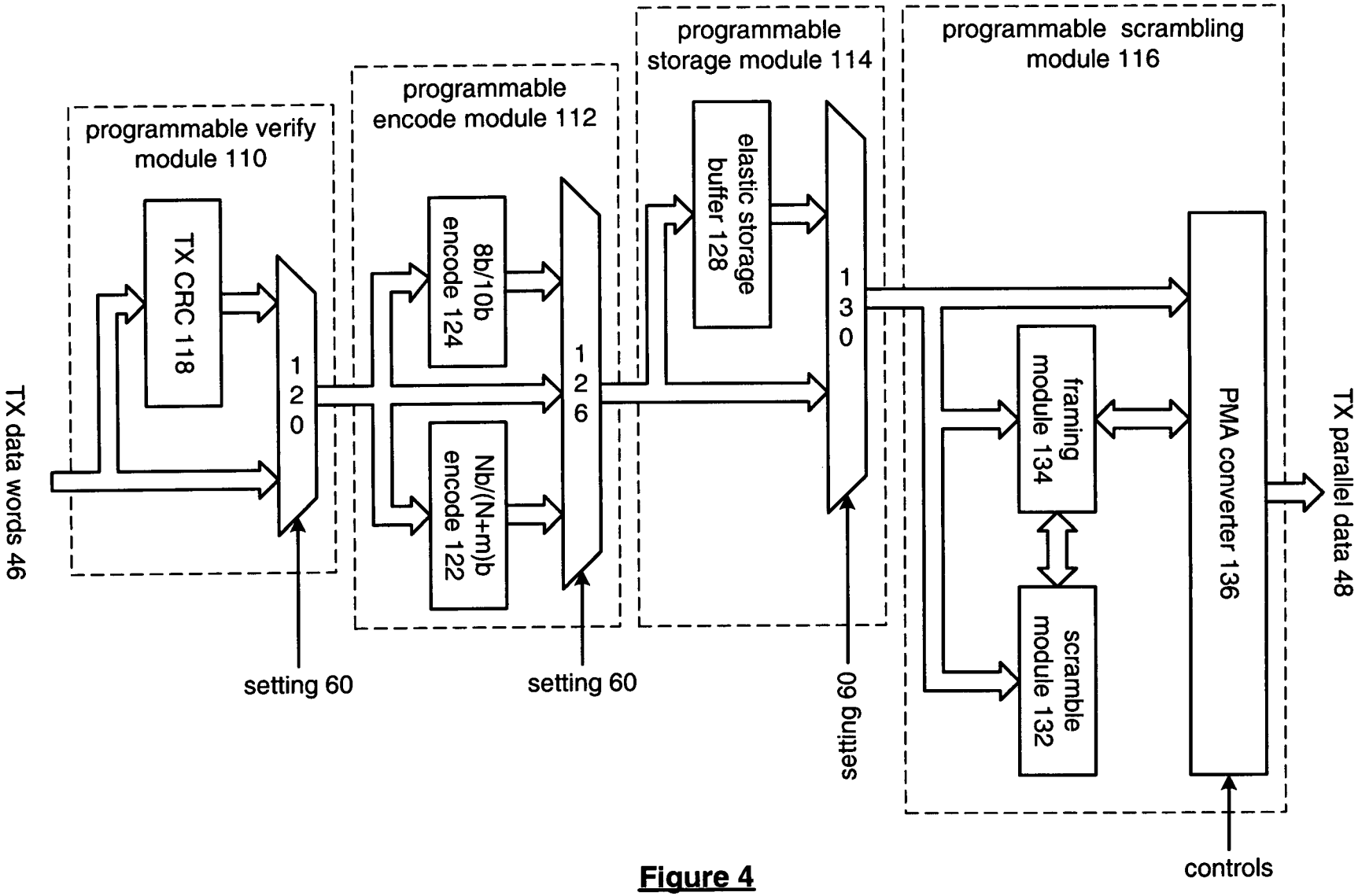


Figure 4
programmabl transmit PCS module 42

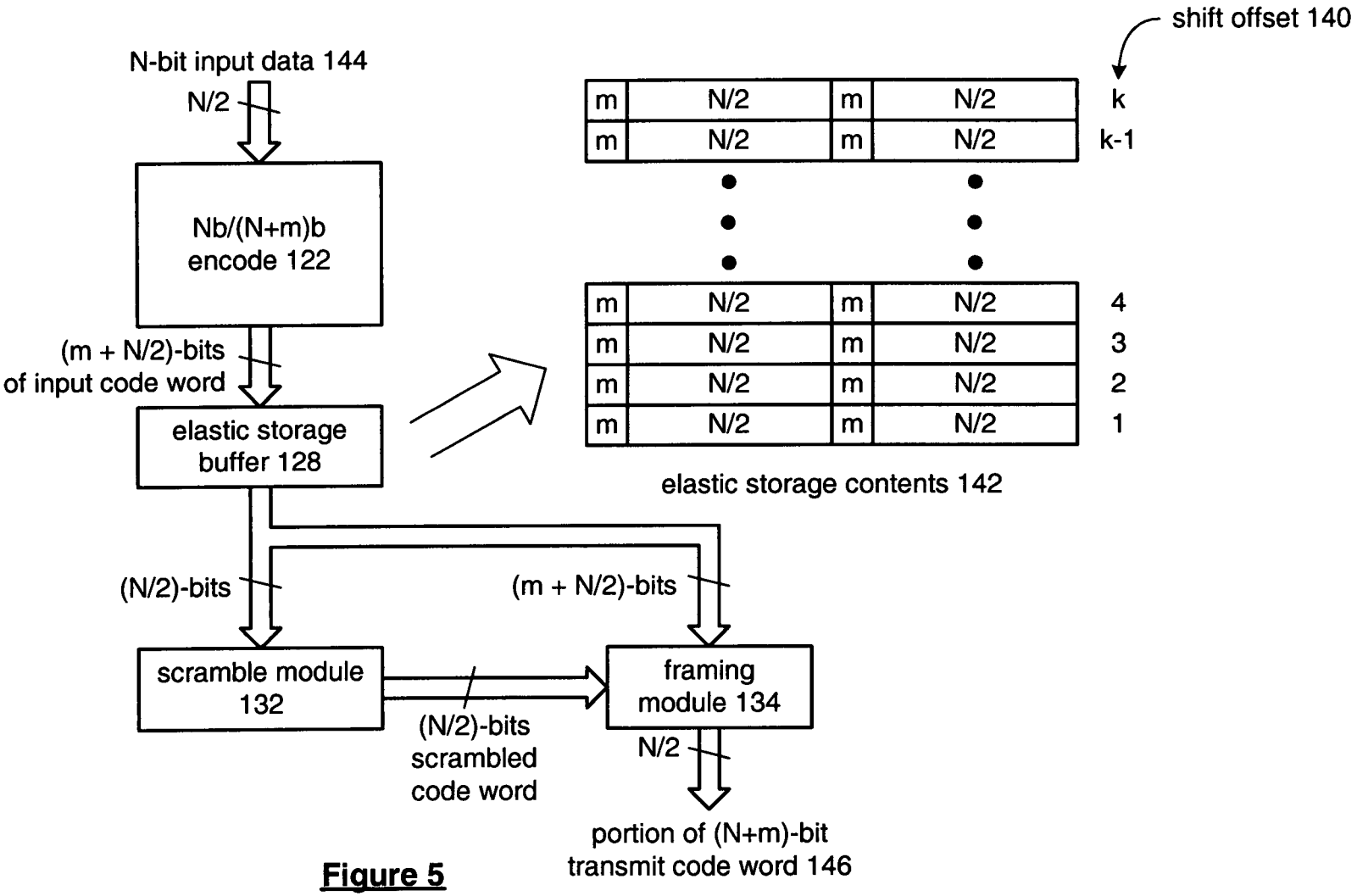
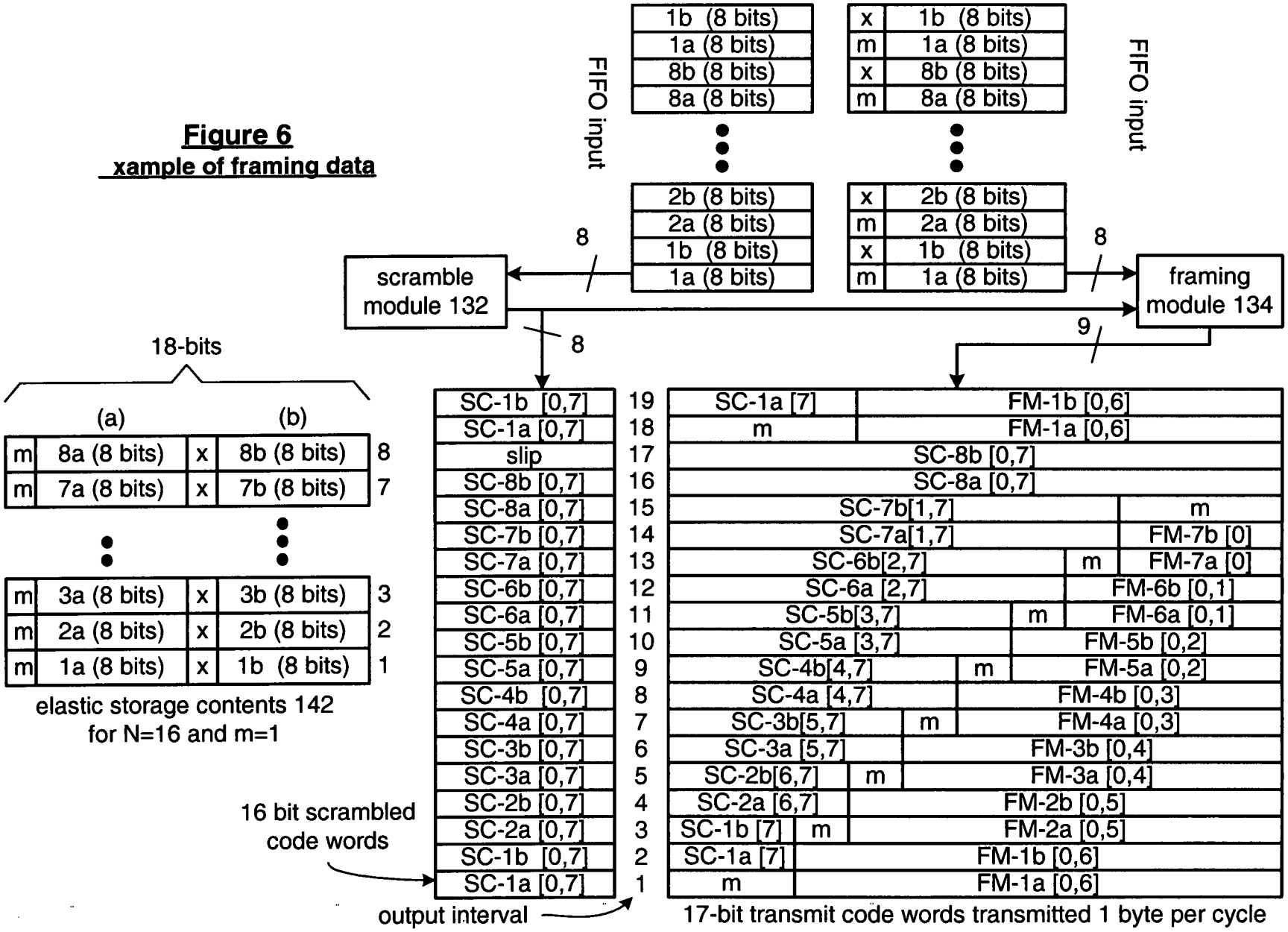


Figure 5

framing ncod d data

Figure 6
xample of framing data



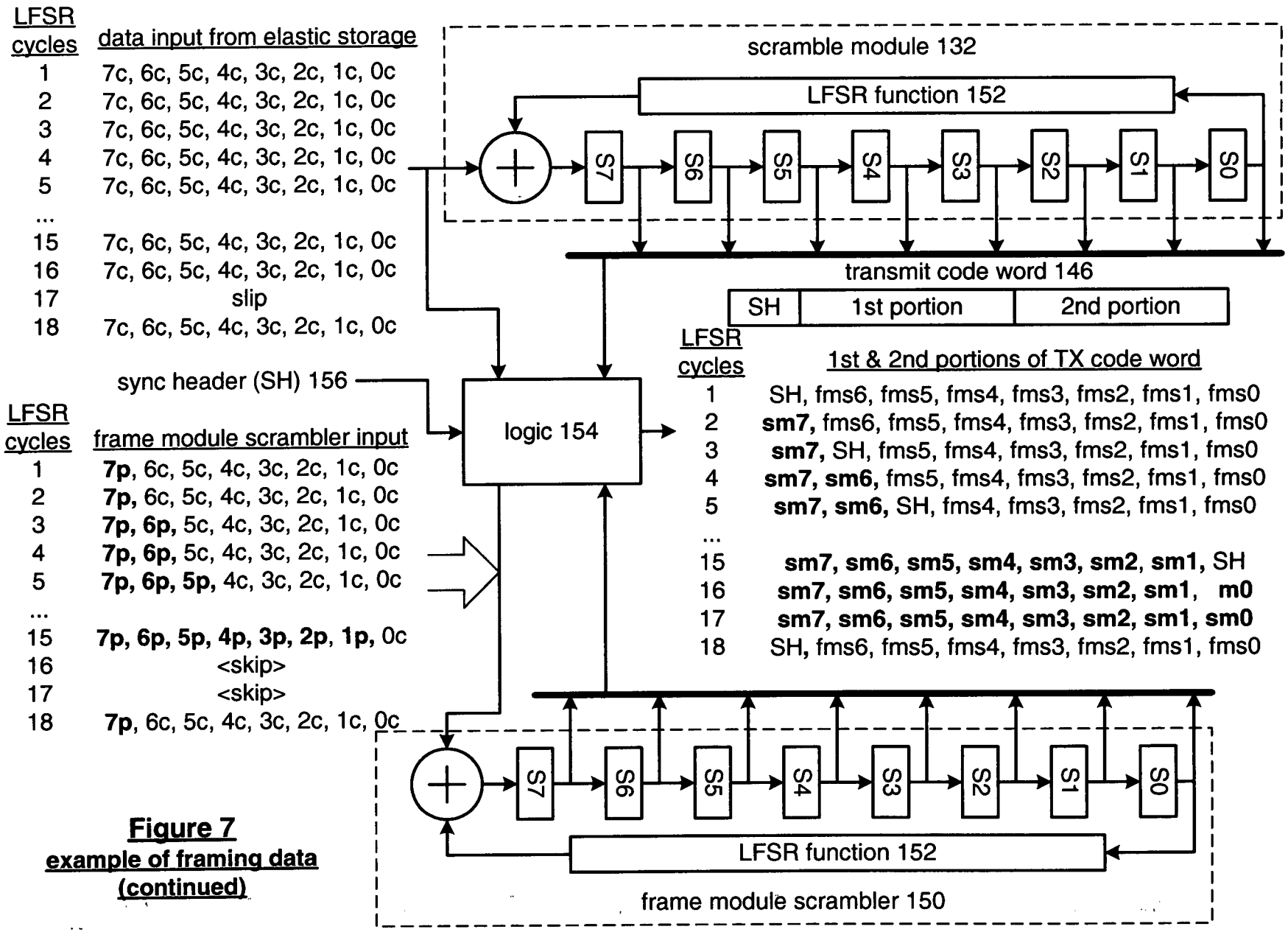


Figure 7
example of framing data (continued)

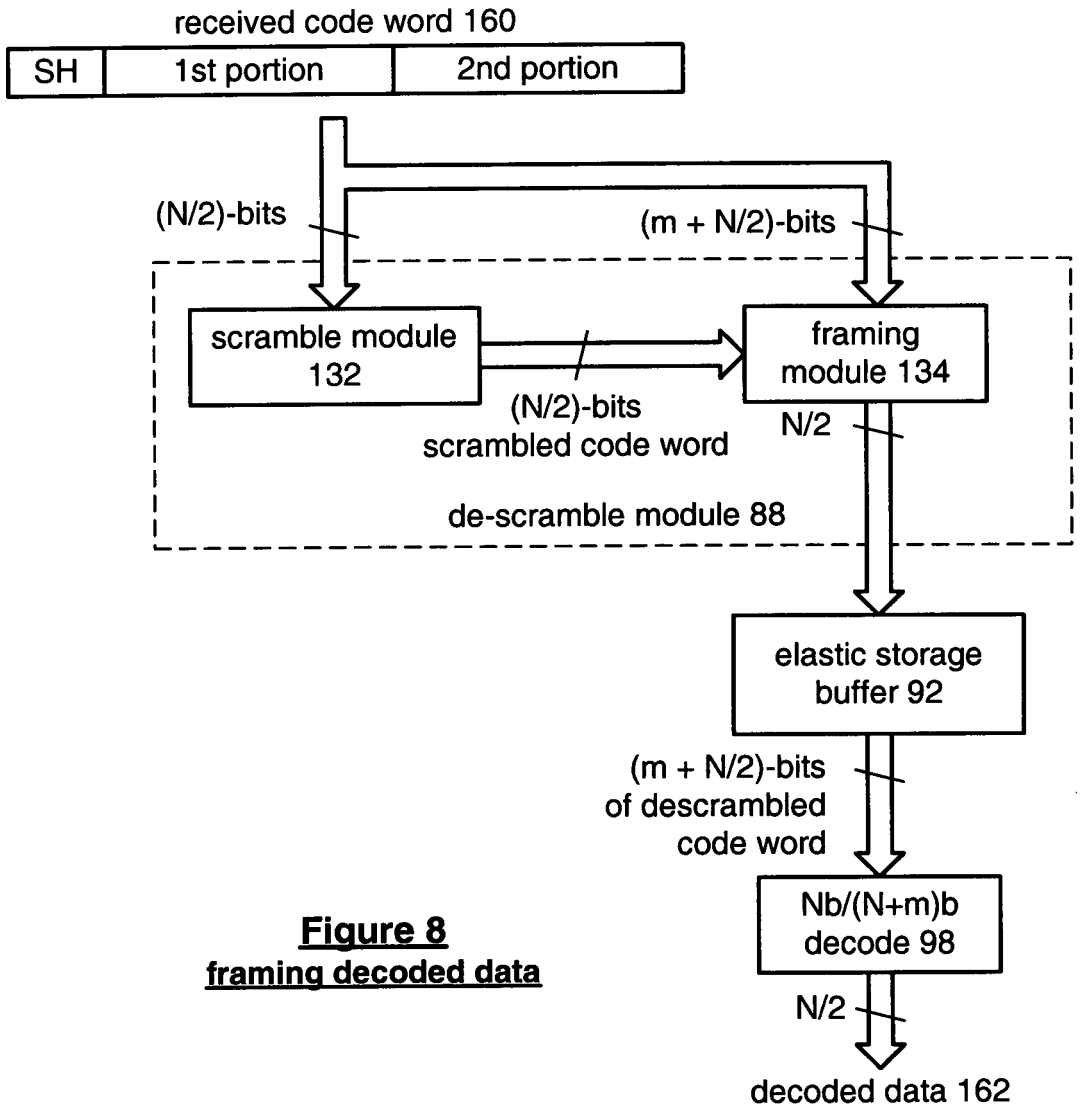


Figure 8
framing decoded data

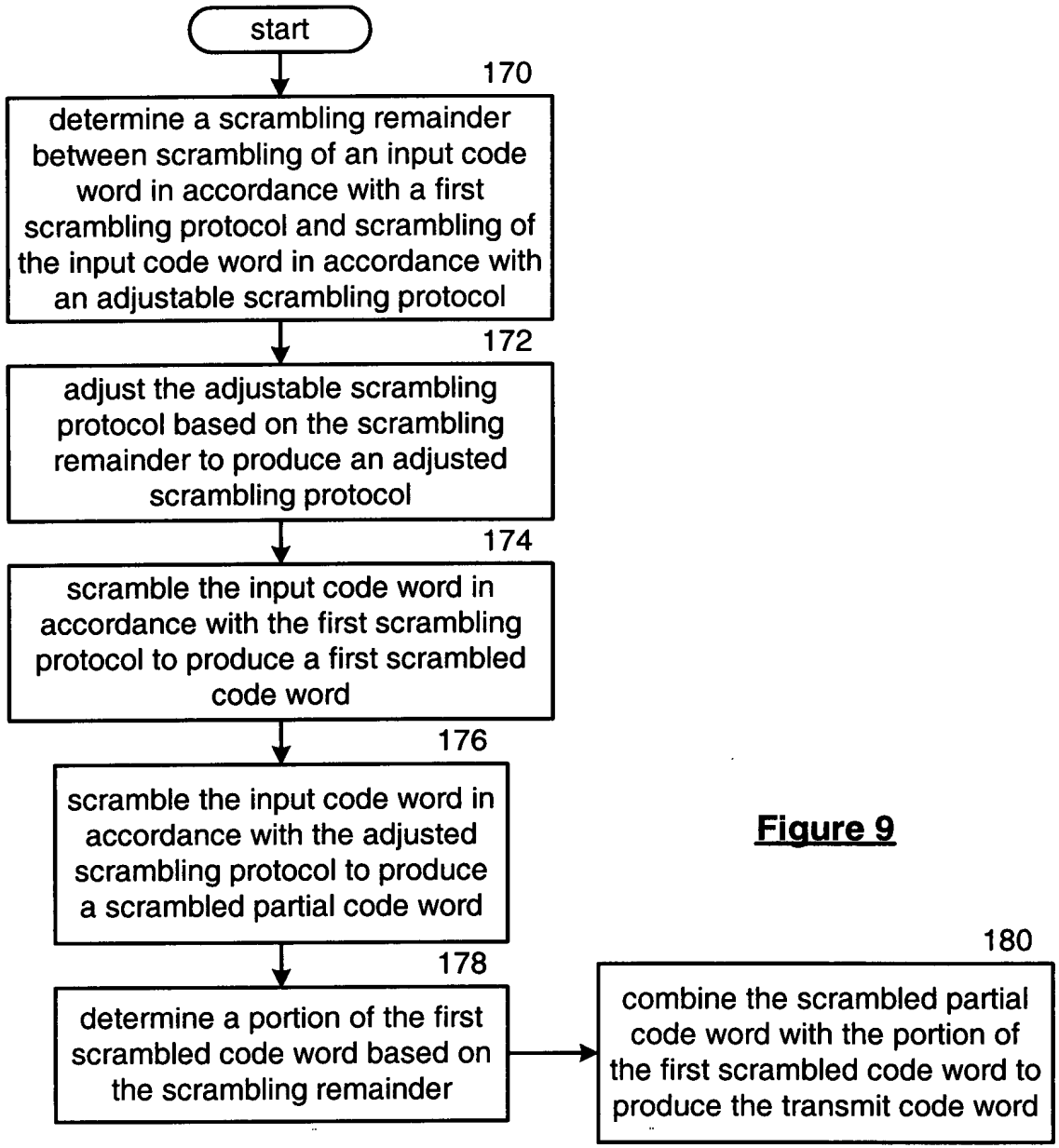

start
170
determine a scrambling remainder between scrambling of an input code word in accordance with a first scrambling protocol and scrambling of the input code word in accordance with an adjustable scrambling protocol
172
adjust the adjustable scrambling protocol based on the scrambling remainder to produce an adjusted scrambling protocol
174
scramble the input code word in accordance with the first scrambling protocol to produce a first scrambled code word
176
scramble the input code word in accordance with the adjusted scrambling protocol to produce a scrambled partial code word
178
determine a portion of the first scrambled code word based on the scrambling remainder
180
combine the scrambled partial code word with the portion of the first scrambled code word to produce the transmit code word

Figure 9

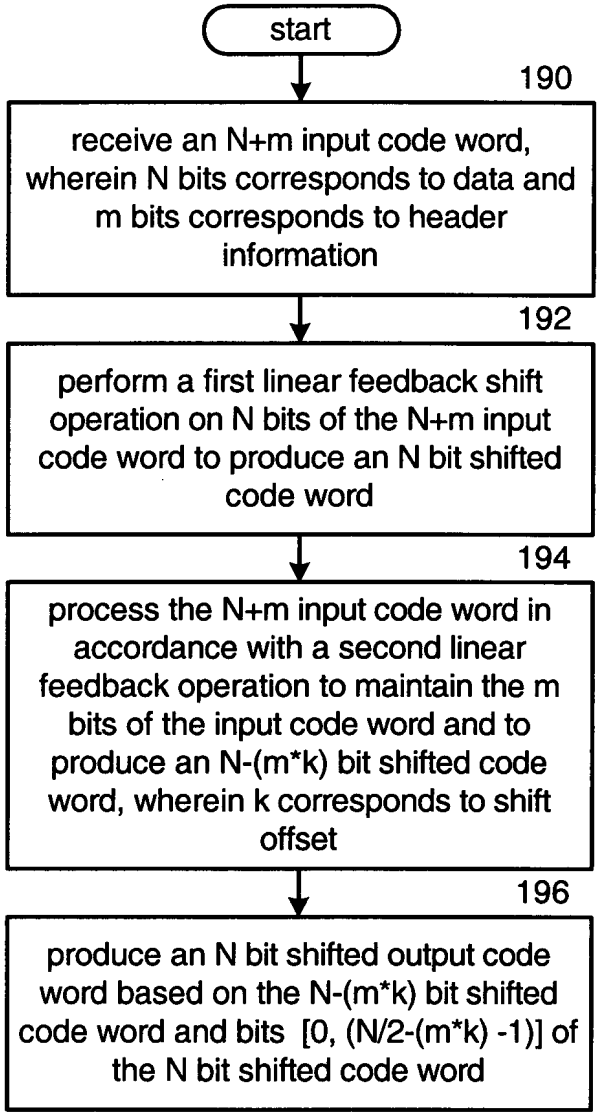

start
190
receive an N+m input code word, wherein N bits corresponds to data and m bits corresponds to header information
192
perform a first linear feedback shift operation on N bits of the N+m input code word to produce an N bit shifted code word
194
process the N+m input code word in accordance with a second linear feedback operation to maintain the m bits of the input code word and to produce an N-(m*k) bit shifted code word, wherein k corresponds to shift offset
196
produce an N bit shifted output code word based on the N-(m*k) bit shifted code word and bits [0, (N/2-(m*k) -1)] of the N bit shifted code word

Figure 10